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☐	L12	(mask$4 near2 (processor or (process$4 adj element)))	1454
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L20: Entry 3 of 9 File: USPT Nov 5, 2002

DOCUMENT-IDENTIFIER: US 6477654 B1
TITLE: Managing VT for reduced power using power setting commands in the instruction stream

Brief Summary Text (10):
In connection with one embodiment of the invention, an application, i.e. a series of instructions to be executed, is recompiled or modified so as to add to the application one or more power control instructions. The power control instructions each may be addressed so as to indicate to which of the functional unit or units that power control instruction applies. The intent is that the power control instructions, after being added to the instruction stream, are stored along with the preexisting instructions so that when the program containing the instructions is executed, the power control instructions will optimize the power status of the plural functional units. More particularly, the functional units which are required for execution of a particular instruction should be in an appropriate power state, that is a high power state at the time the instruction will be executed. Other functional units, which are not required for execution of the particular instruction, need not be in a high power state. In order to add the appropriate power control instructions, an analysis function analyzes the instructions contained in the application to identify correlated functional units. The analysis unit will assume that on initialization all functional units will be in their lowest power state.

Current US Cross Reference Classification (1):
713/322

L20: Entry 4 of 9 File: USPT Apr 9, 2002

DOCUMENT-IDENTIFIER: US 6370651 B1
TITLE: Synchronizing user commands to a microcontroller in a memory device

Brief Summary Text (8):
In such systems, the oscillator circuit can be disabled after the micro controller executes a user command and shuts down. The disabled oscillator circuit halts the micro controller and reduces power consumption of the flash memory device. The oscillator circuit is then re-enabled when a subsequent user command is received. The micro controller restarts and performs the program or erase operation specified by the subsequent user command.

Current US Original Classification (1):
713/322

Current US Cross Reference Classification (1):
713/601

L20: Entry 5 of 9 File: USPT Aug 28, 2001

DOCUMENT-IDENTIFIER: US 6282667 B1
TITLE: Method and apparatus for selectively powering circuitry within a sound device to perform selected sound functions

Brief Summary Text (16):
According to yet still another aspect of the present invention, there is provided a recording medium having program code instructions stored thereon which perform power-supply control in a computer system which has a sound device including various circuits that provide various types of sound functions and an operating system responsive to a request of an application program and capable of issuing an open message to start the execution of a specific type of sound function or a close message to end the execution of the sound function, the instructions comprising: controlling the sound device such that electric power is supplied to the circuits providing the specific type of sound function, when the operating system has issued the open message, and controlling the sound device such that the supply of electric power to the circuits providing the specific type of sound function is stopped, when the operating system has issued the close message.

Current US Cross Reference Classification (1):
713/323

L20: Entry 7 of 9 File: USPT May 11, 1999

DOCUMENT-IDENTIFIER: US 5903746 A
TITLE: Apparatus and method for automatically sequencing clocks in a data processing system when entering or leaving a low power state

Detailed Description Text (27):
In this embodiment, there are 2 low-power modes available. One mode allows only CLKC to be shut down. The other mode allows all clocks to be disabled. These modes are controlled by PLL.sub.-- OFF signal 1108c, ALL.sub.-- OFF signal 1108d, and PLL.sub.-- OK signal 1108e. PLL.sub.-- off signal PLL.sub.-- OFF and all.sub.-- clocks.sub.-- off signal ALL.sub.-- OFF may be formed by circuitry such as illustrated in FIGS. 8 or 10 using a control register such as control register 730 or 930. Once a low power mode is specified by setting a control register, a low power mode is generally not entered until processor 1170 executes an IDLE instruction or writes a bit to a control register to indicate that a low power mode is to be entered. After an all-off low power mode is entered, oscillator enable signal 751 is de-asserted until a wakeup event occurs.

Current US Cross Reference Classification (1):
713/601

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L20: Entry 9 of 9 File: USPT Feb 27, 1996

DOCUMENT-IDENTIFIER: US 5495617 A
TITLE: On demand powering of necesssary portions of execution unit by decoding instruction word field indications which unit is required for execution

Brief Summary Text (11):
As seen from the above, the conventional microprocessor is ordinarily in a condition requiring a substantial consumption of power irrespective of whether the control instruction or the operation instruction is executed, and also, the interrupt instruction is necessary for release of the processor from the standby mode once the processor has entered the standby mode.

Current US Original Classification (1):
713/323

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L20: Entry 2 of 9 File: USPT Sep 23, 2003

DOCUMENT-IDENTIFIER: US 6625740 B1
TITLE: Dynamically activating and deactivating selected circuit blocks of a data processing integrated circuit during execution of instructions according to power code bits appended to selected instructions

Detailed Description Text (28):
The power saving process can be described further by the following brief example. Assume that it takes 10 clock cycles for a component or logic block to transition to the `active` mode from the `sleep` mode and vice a versa. Also assume that each instruction takes one cycle to execute. Therefore, the firmware looks ahead at least 10 instructions to determine which components or circuit blocks are required in the future to execute an upcoming set of instructions and generates the corresponding power control signals. Conversely, if a component or block is required before the next 10 instructions have completed execution, a switch between sleep to active mode is not possible. Additionally, there may be other situations such as jumps, loops or branch conditions where a different set of components or blocks may need activation than those currently active. In such cases, predictive techniques, such as branch prediction may have to be applied or power control simply foregone.

Current US Cross Reference Classification (3):
713/322

CLAIMS:

1. An integrated circuit comprising: a plurality of circuit blocks for selectively performing data processing operations in response to a set of instructions; and circuitry for dynamically activating and deactivating selected ones of said circuit blocks during the execution of said set of instructions in response to power control codes embedded in said set of instructions with bits appended to selected instructions of said set of instructions.

14. A data processing system comprising: a bus for transmitting data; a first processing device for transmitting and receiving data via said bus; and a second processing device for transmitting a receiving data via said bus comprising: a plurality of circuit blocks for selectively performing data processing operations in response to a set of instructions; and circuitry for dynamically activating and deactivating selected ones of said circuit blocks during the execution of said set of instructions in response to power control codes embedded in said set of instructions said control codes comprising bits appended to selected instructions of said set of instructions.

L5: Entry 8 of 75 File: USPT Mar 18, 2003

DOCUMENT-IDENTIFIER: US 6535031 B1
TITLE: Programmable logic integrated circuit devices with low voltage differential signaling capabilities

Detailed Description Text (8):
An illustrative embodiment of LVDS input buffer 70 is shown in more detail in FIG. 2. Buffer 70 is turned on by programing FCE 72 to turn on current sink I1 and current source I2. When buffer 70 is not to be used, FCE 72 is programmed to turn off elements I1 and I2, thereby conserving power that would otherwise be consumed. Buffer 70 is constructed to be able to detect LVDS signals over the full range of permissible voltages according to LVDS standards. In particular, the offset voltage ("Voffset") of the two LVDS input signals INA and INB in FIG. 2 can be anywhere in the range from 0 volts to 2.4 volts when Vcc (power or logic 1 potential) for device 10 is 2.5 volts. Voffset is the average of the voltages of INA and INB. In order to operate satisfactorily over such a wide Voffset range, and especially at Voffset values that can be so close to Vss (ground or logic 0 potential) or Vcc, buffer 70 includes both an NMOS differential stage 100 and a PMOS differential stage 200. The NMOS differential stage includes NMOS transistors 110 and 112 and operates except when Voffset is close to or below Vtn for NMOS transistors (i.e., the gate voltage required to turn on an NMOS transistor). Thus the NMOS stage stops operating or is partially turned off when Voffset is very close to ground potential. The PMOS differential stage includes PMOS transistors 210 and 212 and operates except when Voffset is above Vcc-Vtp (i.e., the voltage below which the gate of a PMOS transistor must be in order for that transistor to turn on). Thus the PMOS stage stops operating or is partially turned off when Voffset is close to Vcc.

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L5: Entry 9 of 75 File: USPT Feb 11, 2003

DOCUMENT-IDENTIFIER: US 6519260 B1
TITLE: Reduced delay priority for comfort noise

Brief Summary Text (5):
As the radiocommunication industry matures, various subscriber usage patterns have been recognized. For example, it has been found that during a typical voice connection between two subscribers, the actual voice activity transmitted over the air interface accounts for less than 50% of the total connection time. Therefore, in an attempt to conserve power, remote units have been designed to actuate the transmission circuitry only during the voice-active portion of a call and render the transmission circuitry inoperative during periods of silence. This has been implemented, for example, using a detector for detecting voice activity and a discontinuous transmitter (DTX) that becomes inoperative when the voice activity detector (VAD) detects a pause in the user's speech. As one skilled in the art will appreciate, this technique has been shown to reduce interference thereby leading to higher system capacity. The DTX technique also reduces power consumption of the remote units by turning off the transmitting circuitry for extended periods of time. Additional information regarding the use of a VAD in a discontinuous transmission system is described in commonly assigned, U.S. Pat. No. 5,881,373 to R. Elofsson et al., entitled "Muting the Microphone in Radiocommunication Systems," the entirety of which is incorporated by reference herein.

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L5: Entry 21 of 75 File: USPT Oct 3, 2000

DOCUMENT-IDENTIFIER: US 6128504 A
TITLE: Apparatus and method of contention resolution for a plurality of handset units in a cordless telephone system

Detailed Description Text (21):
While the handset unit 20 is not being used for communications and is located remote from the base unit 10, the handset unit 20 enters a low power monitoring mode which includes powering down and then powering up certain minimum circuitry in the handset unit 20 as necessary for satisfactory operation. Reducing the on-time state of this circuitry aids in conserving battery power when no communications are in progress between the handset unit and the base unit. Also, other circuitry in the handset unit 20 is turned completely off while the handset unit is in this monitoring mode. In powering down the handset unit 20, the control unit 210 turns itself off or puts itself to sleep and signals the TDD 220 also to turn off while in the powered down state. The control unit 210 also turns off all other clock-driven circuitry in the handset unit 20. After approximately 900 milliseconds, the handset unit 20 is powered up into a minimum power operating state for 100 milliseconds. During the 100 millisecond time period, the control unit 220 turns on and enables the TDD 220, the clock 215 and the receiver portion of the transceiver 230 for determining if an RF signal is being transmitted from the base unit 10 or if a key has been pushed on the keypad in the interface unit and display 265. If neither of these has occurred, the control unit 210 again turns off power to itself and to the TDD 220, and the cycle is repeated. This low power monitoring mode continues as long as an RF signal is not received from the base unit 10 or a key has not been pushed on the keypad.

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L3: Entry 1 of 1 File: TDBD Sep 1, 1986

DOCUMENT-IDENTIFIER: NN86091723
TITLE: Method of Power On/Off Diskette Controller

Disclosure Text (1):
- A CMOS diskette controller that is program compatible with the IBM Personal Computer (PC) diskette controller is not available. In building a battery-powered portable PC that is program compatible with the existing PC line, a NMOS diskette controller had to be used. To conserve battery power, this controller's power must be turned off when the diskette drives are not being accessed. A method is described to solve this problem without sacrificing program compatibility. The program never knows that power is being cycled on the diskette controller even if the program goes around the PC BIOS microcode. This method involves both microcode and hardware. The normal state of the diskette controller is power off. When a program accesses one of the diskette controller ports with either a read or write I/O, a Non-Maskable Interrupt (NMI) is generated. This activates ROM microcode that powers on the controller and issues I/O commands to the controller to re-synchronize its state with the state of the diskette drives. This re-synchronization process consists of re-initializing diskette drive parameters kept by the controller as well as re-establishing the current head position of each drive that is attached to the controller. Once this has been done, the NMI microcode decrements the program return address on the stack by one, restores all registers, and returns to the program that issued the I/O instruction while the controller was in the off state. Since the return address was modified by one, the original IN or OUT I/O instruction is reissued to a powered on, updated controller. The controller power stays on until the diskette motor's transition to an off state. The hardware then powers off the controller. The hardware is designed so that switching from one drive motor to another does not power off the controller. This insures that there is no NMI generated and no performance degradation when doing copy operations between drives. In most microcode accesses to the diskette system, the diskette drive motors are turned on before the controller is accessed. Since a 500-millisecond delay is required for motor start-up before accessing the diskette drive, the controller power-up sequence is overlapped with this delay, adding no additional time to the diskette access. The hardware support for this function consists of the following: 1. A circuit which decodes I/O commands to a powered-off diskette controller and generates a Non-Maskable Interrupt. 2. A circuit controlling the power to the diskette controller. This circuit powers on the controller in response to a new I/O command decode. The circuit also powers the controller off when the motor-enable signals to the diskette drives transition from on to off. 3. A Head Position Counter for each drive is provided to maintain the head position information for each drive independent of the controller. The circuit uses the Drive Select, Direction and Step signals to the Drive and the Track 0 signal from the drive to control the position counters. 4. Circuitry is provided to logically disconnect the controller signals to the diskette drives, so that the controller may be re-synchronized after a power on without affecting the state of the diskette drives. This circuit also provides a false Track 0 indicator to the controller to aid in the controller re-synchronization sequence (specifically the Recalibrate command). The microcode consists of the NMI handler routine that is activated by an I/O access to the controller when it is in the power-off state. The

following operations are performed by this routine: 1. All drives are temporarily deselected. 2. Activate Diskette Controller Power. 3. Reset the diskette controller. 4. Read all drive head position counters. 5. Issue specify command (for step times and head settling). 6. Issue overlapped recalibrate commands for all drives. 7. Wait for operation complete. 8. Issue overlapped seek commands for each drive to the position indicated by the track counters read above. 9. Wait for operations complete. 10. Set the drive select signals back to the value on NMI entry. 11. Decrement the NMI program return address on the stack by 1. 12. Return from the NMI routine to the program. The above sequence will re-establish the controller state without the program being aware that the controller was at first powered off. Decrementing the return address by 1 to re-execute the I/O command to the controller is always correct due to the fact that the IN AL,DX and the OUT DX,Al instructions are one-byte instructions and the NMI always occurs immediately after the instruction has executed.

L9: Entry 1 of 3 File: USPT Mar 27, 2001

DOCUMENT-IDENTIFIER: US 6206108 B1
TITLE: Drilling system with integrated bottom hole assembly

CLAIMS:

7. The bottom hole assembly of claim 1, wherein the processor turns on and turns off sensors in the BHA according to a predetermined selection criteria, thereby conserving power and increasing the operating life of such sensors.

L9: Entry 2 of 3 File: USPT Jul 11, 1995

DOCUMENT-IDENTIFIER: US 5432578 A
TITLE: Illuminating device for a camera

CLAIMS:

11. An illuminating device for a camera having an illuminating element which illuminates a display device which displays information related to photography, a release actuation device which upon a first stroke outputs a half press signal to begin preparation for photography and upon a second stroke exceeding said first stroke outputs a full press signal to begin a photographic operation, and a mode actuation device which is operated for setting a mode related to photography and outputs a mode command signal according to the mode setting, comprising:

a photometric device the operation of which is started when said mode command signal is output from said mode actuation device and which measures the luminance of a photographic subject;

a signal output circuit which outputs a turn on signal when the luminance measured by said photometric device is less than a predetermined value;

a timing circuit which outputs a turn-off command signal after a predetermined time period has elapsed from the turning on of said illuminating element; and

a control circuit which turns on said illuminating element according to said turn on signal, and turns off said illuminating element to conserve power according to the earlier one of said turn-off command signal and the half press signal input to said control circuit from said timing circuit and from said release actuation device; and

a turn on actuation member which is operated to output said turn on signal.

L5: Entry 2 of 75 File: USPT Nov 18, 2003

DOCUMENT-IDENTIFIER: US 6648821 B2
TITLE: Microprocessor controlled ambulatory medical apparatus with hand held communication device

Detailed Description Text (215):
When there is no inter-processor communication active, the software running in each processor IC turns off the clock to SSI-A to conserve power.

L5: Entry 4 of 75 File: USPT Aug 19, 2003

DOCUMENT-IDENTIFIER: US 6609193 B1

**** See image for Certificate of Correction ****

TITLE: Method and apparatus for multi-thread pipelined instruction decoder

Brief Summary Text (7):

In processors, reducing power consumption is an important consideration. In order to conserve power in prior art processors, entire functional blocks of synchronous circuitry within the execution unit have their clocks turned OFF. That is, their clock signals are set to a stable state throughout entire functional blocks. In order to accomplish this, prior art power down control logic was used to determine when an entire functional block is idle and can have its clocks shut off. By shutting the clocks OFF to synchronous circuits, signals, including the clock signal, do not change state. In which case transistors are not required to charge or discharge capacitance associated with the signal lines and therefore power is conserved. However, because the clocks are shut OFF throughout entire functional blocks, the prior art processor has to wait until all functions are completed within such blocks. This causes the prior art processor to rarely shut OFF clocks to the functional blocks such that little power is conserved over time.

L22: Entry 4 of 17 File: USPT Nov 16, 1999

DOCUMENT-IDENTIFIER: US 5987244 A
TITLE: Power management masked clock circuitry, systems and methods

Detailed Description Text (52):
A DOS-compatible static 486 core in MPU 102 allows on-the-fly clock-scale and clock-stop operation to conserve battery power. The special clocking scheme allows optional clock stopping between keystrokes. Low voltage operation such as 3.3 volts or less, coupled with power management, provides the capability to achieve low system battery power consumption. Bus 104 is a high speed high bandwidth bus to improve data transfers of bandwidth-intensive I/O devices such as video. Electrical noise is minimized by this embodiment which has short conductor trace lengths and direct point-to-point clock traces. Each clock trace has a series or parallel termination to prevent undesirable reflections. An economical 74LS244 clock driver 180 is provided in the interior of quadrilateral 303. Placement of that clock driver 180 is such that the length of the clock traces therefrom to each chip 110, 102, 114 and 112 are approximately equal, advantageously minimizing clock skew.

Detailed Description Text (536):
In Suspend Mode, assertion ofthe SUSPEND input (hsuspendx) pin signal to MPU 102 in FIG. 33 not only masks the core processor 702 clock via gate 3610, but also PCI bridge and memory controller MCU 718 have their respective clocks hclk2, hclk maskes as well as clock outputs (PCLKOUT and NPUCLK) by further advantageously clock gates 3622 and 3624 in pair 3620. Beforehand internal MPU block 718 of FIG. 33 acknowledges (by signal hstopfmmcu) that it can stop, whereupon signal hstoposc is generated and the clock outputs from gates 3620 are stopped by control signal ENX of FIGS. 34 and 36. When SUSPEND is deasserted, the suspend mode is terminated and the oscillator is enabled by control signal hresume. After a short time, the clock signals to the MPU 102 are restarted and Pll 706 restarts. Stability and duty cycle requirements are maintained for all clocks during transitions into and out of suspend mode.

Detailed Description Text (955):
The STANDBY state conserves power by adjusting CPU turn-on time by a Mask Clock circuit of FIG. 27.

Current US Cross Reference Classification (1):
713/601